a channel region having the second conductive type and disposed on the drift region;

a gate region surrounding at least a part of the channel region via an insulation film, the gate region having the first conductive type;

a source region having the second conductive type provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film; and

a source electrode connected to the source region,

wherein a depletion layer is formed over most of the entire channel region when a predetermined voltage is applied to the gate region.

4. (Twice Amended) The semiconductor device according to claim 1, further comprising a semiconductor region having the first conductive type and provided between the channel region and the source electrode.

12. (Four Times Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a second conductive type different from the first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the first conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film, wherein:

mixing 2 embodiments 112 1st together. P. 8 figs. 8A, 8B

[an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region].

04 F 112 1st Sub A1

22. (Amended) The semiconductor device according to claim 12, wherein:

the gate region has the first conductive type.

05 F

23. (Amended) The semiconductor device according to claim 22, further comprising a source electrode provided on the source region.

Sub G2 fig. 8 06

26. (Amended) The semiconductor device according to claim 12, further comprising a semiconductor layer having the first conductive type located between the source region and the source electrode, the semiconductor layer including an end face extended to a position covering at least a portion of the gate region.

Subt F-2

112 1st F 07

28. (Amended) The semiconductor device according to claim 26, further comprising an insulation layer located between the semiconductor layer and the source electrode and having an opening portion for the semiconductor layer and the source electrode to contact, wherein a width of the opening portion is wider than [a distance 112 2nd of the gate region].

Subt F-3

112 1st F 08

29. (Amended) The semiconductor device according to claim 27, further comprising an insulation layer located between the semiconductor layer and the source electrode, and having an opening portion for the semiconductor layer and the source electrode to contact, wherein a width of the opening portion is wider than [a space 112 2nd of the gate region].

Subt F-4

112 1st F 09

30. (Amended) A semiconductor device comprising:

[a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a first conductive type and provided on the drift region;